Advances in High Rate Silicon and Oxide Etching using ICP

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Abstract:
This paper presents the latest developments in high rate deep silicon and oxide etching for MEMS applications. Investigations into the rate limiting step for silicon etching show that the radical flux density is the most critical parameter. Ion density, ion energy and wafer temperature do not play any significant role in enhancing the etch rate. Etch rate enhancement nominally by a factor of 2 is reported as a result of radical flux increase. Results are also presented for a new ICP dielectric etch source, with etch depth capability exceeding 100 μm.

Introduction:
Silicon and silicon dioxide (quartz, glass, etc.) are the most commonly used materials for the fabrication of MEMS devices, together comprising over 95% of the substrates used. MEMS development laboratories have made demonstrator devices covering a vast number of micro sensor and actuator applications. However the move from lab scale to volume manufacture has been much slower than anticipated. The main reasons for this center around back-end packaging, front-end device yield and the overall device cost versus performance issues. Defining the device structures necessitates etching of the substrate materials and higher transducer performance can require deeper and higher aspect ratio etching. Etch rate is inevitably one of the commercial factors affecting feasibility of volume manufacture of a large number of the devices in the MEMS emerging market. This paper focuses on recent advances in high rate etching of both silicon and silicon dioxide using inductively coupled plasma systems.

1. High Rate Silicon Etching:

The STS Advanced Silicon Etch (ASE®) process is based on the cyclic etch/passivation method of anisotropically etching silicon invented by Lärmer and Schilp [1]. The ASE® process allows high rates, anisotropic profiles with high selectivity to conventional photoresist masks[2]. The mechanistic details of the ASE® process have been introduced elsewhere [2]. Essentially SF_6 is used during an etch step to etch Si isotropically, this is followed by a short passivation step using C_4F_8 and the steps are alternately repeated. The passivation protects the sidewall of the feature from etching, thereby allowing anisotropy to be maintained.

The apparatus and basic characteristics have previously been detailed [2,3,4]. Investigations have been carried out into the rate limiting factors focusing on parameters such as the plasma density, ion bombardment energy, wafer temperature and the radical species. The following results were obtained for the etch step only. The basic process conditions used were: SF_6 flow rate 130sccm, RF coil power 800W, wafer electrode temperature 10°C, RF bias 3W and chamber pressure 35mTorr. The 100mm test wafers were patterned with positive photoresist (with no post bake) to yield a silicon exposed area of >95%. Figure 1 shows the effect of RF bias power on the mean etch rate. Clearly the bias (which determines the ion energy) has no influence on etch rate. Figure 2 shows the etch-rate variation with coil RF power at various SF_6 flow rates and pressure values. The results show that etch rate increases with both flow rate and pressure. Furthermore, at low flow rates, the etch rate saturates with increasing coil power. Indeed, etch rate has been doubled by increasing the ICP source power at higher gas flows and at increased pressure. Raising the ICP source power has the effect of increasing both the F radical density and the ion density. In order to decouple the two effects, the source to wafer distance was also studied. Figure 3 shows its influence on etch rate for 130 sccm SF_6 at 800W and 3000W coil powers. The data shows no strong interaction. As the distance of the wafer increases from the source, the plasma density will decrease (as there is no magnetic confinement). Other changes with

distance will include, reduction in short lifetime species (due to increased recombination losses) and a reduction in joule heating of the wafer. To negate the relative effcets of wafer heating, the wafer temperature influence was independently studied over a comparative range. The electrode temperature was directly measured by using thermocouples and correlation to the wafer temperature was achieved by using sensitive adhesive labels on the front surface of the wafer.

At 260 scccm SF_6 flow rate, 35 mTorr and 3000W, figure 4 shows the silicon etch rate as a function of electrode temperature, clearly showing no direct dependence. Therefore the results suggest that moderate variations in ion density, wafer temperature, and short lifetime species do not play a significant role in the etch process. Hence it is concluded that the main rate-limiting step is the concentration of F radical species available to etch silicon to form volatile SiF_x. Figures 5, 6a and 6b show SEMs of silicon trenches etched under high rate ASE® process conditions, notably at 260 scccm SF_6 flow rate, 35 mTorr and 3000W coil power. Note in both cases etch rate increase has not been detrimental to parameters such as profile control etc. The etch rate is a strong function of exposed area of silicon, being inversely proportional. Hence etch rate must be defined for wafer size, exposed area, the feature size range and the etch depth.

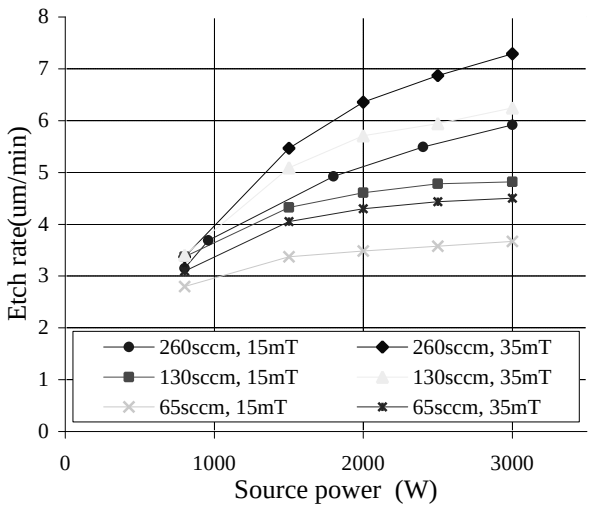

Figure 2. Etch-rate variation with ICP RF power, SF_6 flow-rate and pressure.

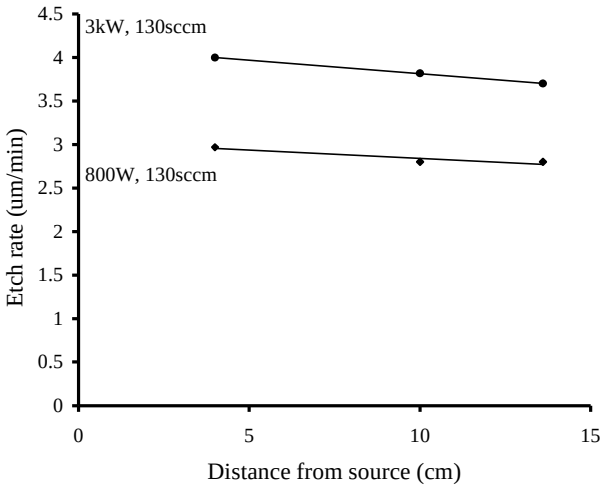

Figure 3. Etch Rate versus wafer distance from ICP source.

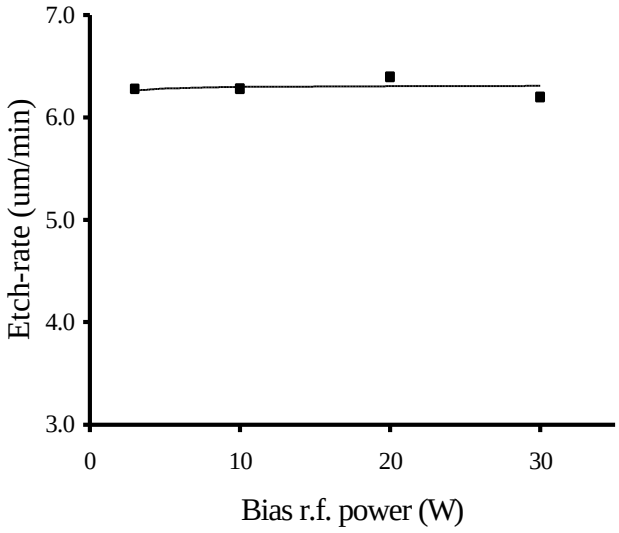

Figure 1. Etch Rate as a function of RF Bias.

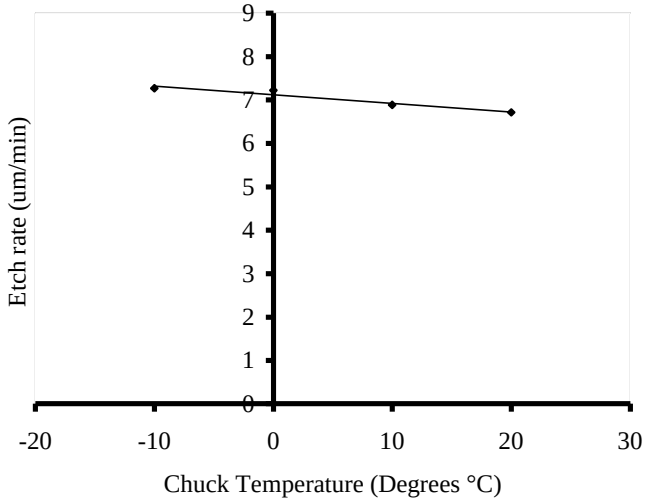

Figure 4. Etch Rate versus electrode temperature.

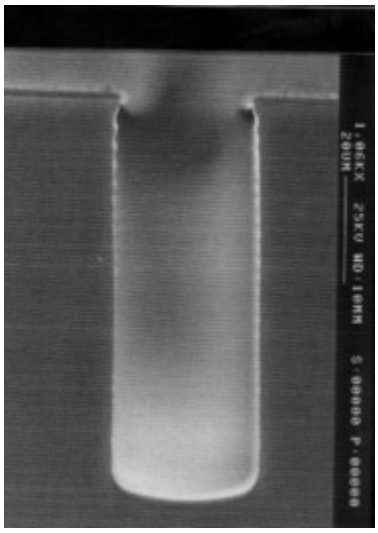

Figure 5. SEM of 25µm trenches etched at >7.5µm/min. Exposed Si area on 100mm diameter <20%

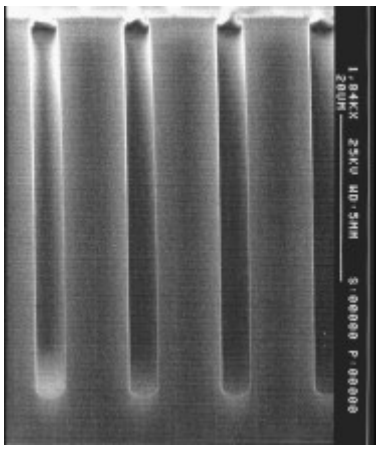

Figure 6a. SEM of 50µm smooth walled trenches etched at 0.8µm/min using 800W coil power. Exposed Si area on 100mm diameter <20%

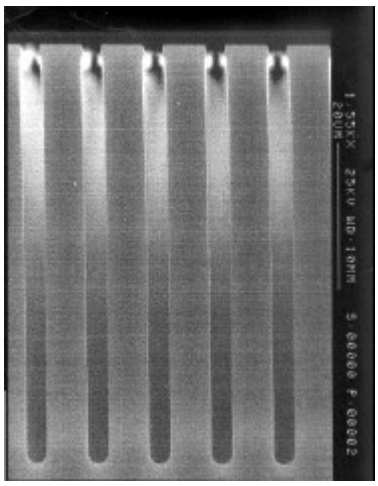

Figure 6b. SEM of 50µm smooth walled trenches etched at 1.9µm/min using 3000W coil power. Exposed Si area on 100mm diameter <20%

2. High Rate Oxide Etching:

Conventional RIE (RF diode and triode plasma systems) are commonly used to etch thin oxide films in the silicon industry. Where either high etch rate, high selectivity and/or high aspect ratio (HAR) processing is needed, HDP tools are being adopted. These systems operate at lower pressure (a few mTorr versus several hundred mTorr) as well as maintaining an ion density up to 10^{12} cm^{-3} which is up to a factor of 100 higher. Much has been published over the last few years on the ability of HDP tools to meet HAR processing at high etch rates and high selectivities to the mask and/or underlayers [5]. However, while these tools are suitable in meeting the needs of advanced thin film etching, they notably require frequent chamber cleaning to maintain etch performance. Thus for thick oxide etch applications (greater than several microns), the high clean frequency begins to seriously erode the tool throughput. Indeed the tools become totally unsuitable when the etch depth requirement is several tens of microns as this can exceed the mean time between cleans (MTBC) for some HDP tools. As there is a trade off between the selectivity and clean frequency, the problem becomes particularly acute when high selectivities are necessary. An increasing number of MEMS and opto-electronic applications fall into this definition.

In order to understand the cause of the relatively high chamber clean frequency, we need to consider the etch mechanism in detail. The basic oxide etch process is has been extensively covered in the literature [6]. The mechanistic details are discussed in terms of the C:F ratio (to control selectivity) and the key role played by surface ion bombardment. More recently attention has focused on the radical ratios (CF_3:CF_2:CF:F) [7]. In HDP systems, the higher electron density results in a corresponding increase in the fragmentation of the precursors. This in turn changes both the simple C:F ratio as well as the more complex radical ratio compared to that of the lower density diode and triode systems. The net result is that higher molecular weight fluoro-carbon precursors are used in HDP tools to re-balance the critical ratios at the wafer surface. Precursor C:F ratios are typically increased by a factor of 2 (for example changing from CF_4 to C_4F_8). Increased H_2 additions are

also commonly used which further reduce the F levels. The consequence of this change is increased deposition on all areas of the reactor furniture, which becomes the cause of the high frequency of chamber cleans.

In order to overcome this inherent limitation, STS has designed an advanced oxide etch (AOE) system. It comprises a completely new ICP source design based on a patent pending coil arrangement with multipolar magnetic confinement at the chamber sidewalls, as illustrated schematically in figure 7.

The following results present part of the tool characterization data for deep oxide etch MEMS (including waveguide etch) applications. The precursor gases comprised $C_4F_8/Ar/H_2$. The basic process conditions used were: $C_4F_8/Ar/H_2$ flow rate 100sccm, RF coil power 1000 W, wafer electrode temperature 10^oC, RF bias 300W and chamber pressure 3 mTorr. Test wafers comprised 100mm silicon with either 6 to 40μm PECVD undoped oxide, patterned with an undoped polysilicon or amorphous silicon mask, or thinner oxide patterned with a positive photoresist mask (post baked at 100 ^oC). Figure 8 shows the etch rate of oxide as a function of H_2 addition to the C_4F_8/Ar. The rate decreases by 12% for up to 20% H_2. Figure 9 shows the corresponding selectivities to resist and undoped polysilicon.

Figures 10 and 11 show 8μm and 40μm thick PECVD oxide etched waveguide cores at rates of 0.4μm /min, selectivity to polysilicon mask >25:1 and etched sidewall angle >89^o. Figure 12 shows a 0.1μm critical dimension feature etched in a 0.2μm oxide layer, at similar etch rate and silicon selectivity values. In all cases the etch uniformity was within $\pm$ 2% [(max-min)/2mean].

Deep etching (approximately 100μm) experiments were carried out using a Ni mask. Here at high etch selectivities to the mask, etch rates exceeding 0.5μm/min were obtained, refer to figure 13.

Turning our attention to the clean frequency of the AOE system, which is the major drawback of the preceding generation of HDP sources, experiments were carried out to establish the clean frequency compared to a cylindrical dielectric window (CDW) type of ICP with a side antenna as opposed to the top antenna of the AOE. A simulation of 2500 wafer microns of oxide etching was carried out for both systems. The results are shown in figure 14 under similar performance figures for the two ICP systems in terms of etch rate (0.35 μm/min) and high mask selectivity. The data shows that the CDW ICP source required cleaning within a hundred wafer microns, while the AOE source resulted in an increase in the clean interval by a factor of >10. In other words, the AOE has only 10% of the MTBC of the CDW ICP source.

Typically, the AOE has up to 10 times longer MTBC than the CDW ICP. As the cleaning time accounts for >50% of the scheduled downtime, the AOE effectively yields >80% reduction in the scheduled downtime, which can increase the uptime by more than 10%. This shows how the new technology can have a significant impact on the cost per wafer. Moreover as etch depths go over several tens of microns, only the AOE is able to meet performance requirements. This factor differentiates this new source as an enabling technology. Table 1 defines the deep etch specification for the new AOE.

Conclusions:

Investigations into high rate anisotropic silicon etching have shown that the radical concentration is the rate limiting parameter. By increasing the radical flux to the wafer (operating at higher ICP power and at higher etch precursor flow rates) rate increases nominally by a factor of two have been obtained.

The new AOE source has clear benefits over conventional HDP oxide etch technology, allowing relatively high etch rates and selectivities to be realised without negatively impacting on the deposit accumulation on the chamber furniture. This results in an ability to carry out deep oxide etching (over 100μm) as well as reducing the clean frequency and hence the cost per wafer. This enables MEMS manufacturers to exploit applications which up until now, have been limited by the available technology.

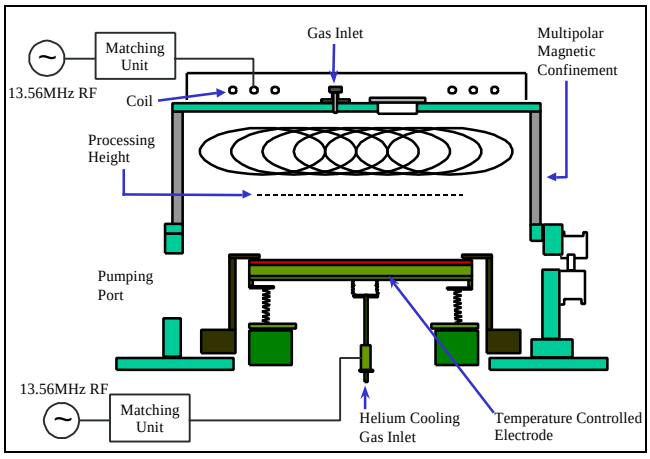

Figure 7. Schematic of new ICP source.

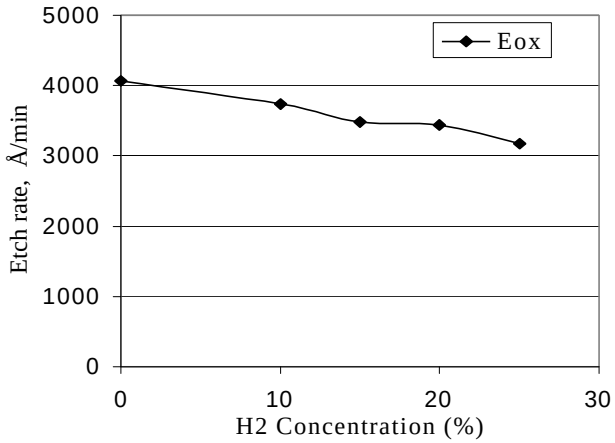

Figure 8. Etch rate of oxide as a function of H_2 addition to the C_4F_8/Ar.

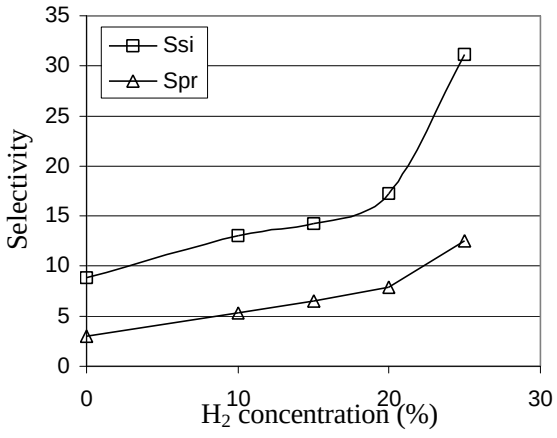

Figure 9. Selectivity to resist and polysilicon as a function of H_2 addition to the C_4F_8/Ar.

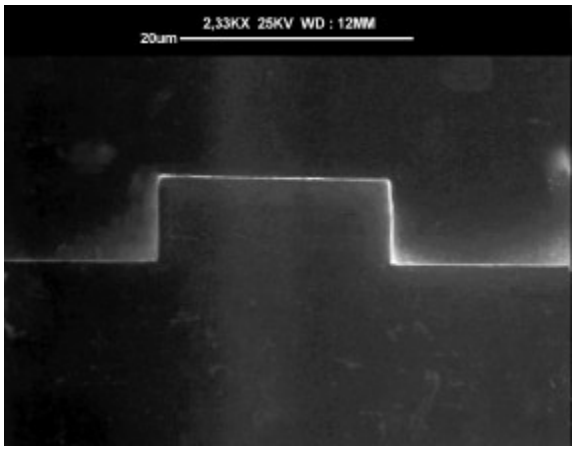

Figure 10: 8μm depth waveguide core etch

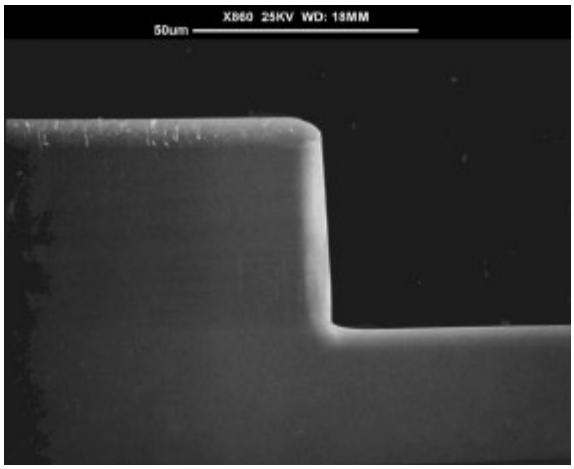

Figure 11: 40μm depth waveguide core etch

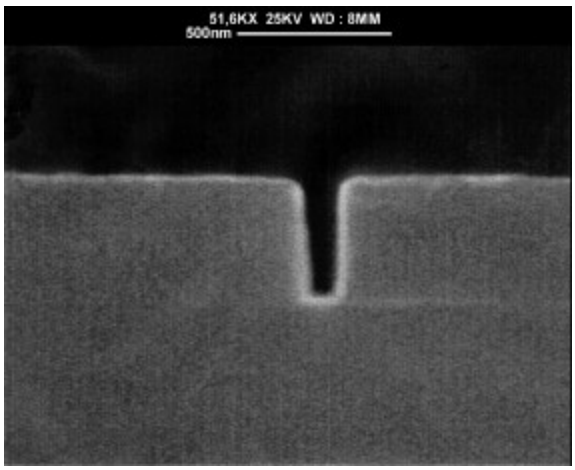

Figure 12: Shallow oxide etch with a 0.1μm CD.

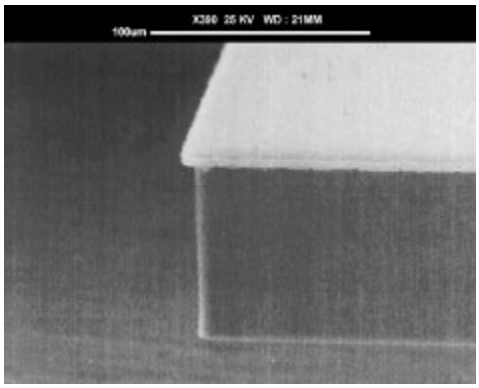

Figure 13: 95 µm deep quartz etch

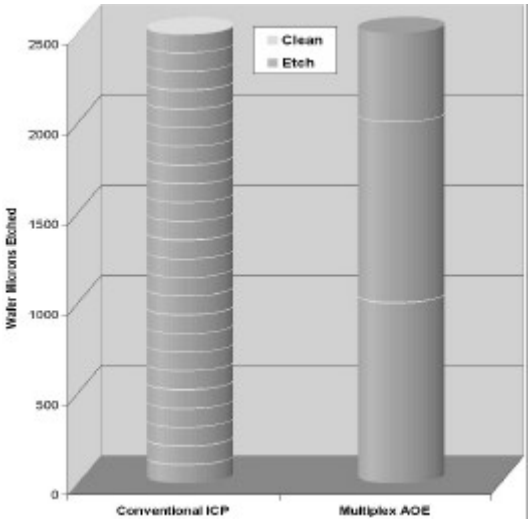

Figure 14. Comparison between clean frequency for CDW ICP and the AOE source

Typical Specifications	
Etch rate:	**0.3 - 0.5 µm/min**
Selectivity to photoresist:	**>10:1**
Selectivity to polysilicon:	**up to 25:1**
Profile *:	**>89º**
Uniformity:	**<±2% X- wafer** **<±2% wafer - wafer**
Clean Frequency:	**>1000 wafer microns**

Table 1. Typical process specifications for AOE source (*assumes mask profile >88º).

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Acknowledgments:

The authors acknowledge the courtesy of SiTek Inc. for their permission to use the micrograph shown in Figure 13.